A Si-Compatible Fabrication Process for Scaled Self-Aligned InGaAs FinFETs

A. Vardi, *Member, IEEE*, J. Lin, *Member, IEEE*, W. Lu, *Student Member, IEEE*, X. Zhao, *Student Member, IEEE*, A. Fernando-Saavedra, and J. A. del Alamo, *Fellow, IEEE*

***Abstract*—We have developed a scalable gate-last process to fabricate self-aligned InGaAs FinFETs that relies on extensive use of dry etch. The process involves F-based dry etching of refractory metal ohmic contacts that are formed early in the process. The fins are etched in a novel inductive coupled plasma process using $BCl_3/SiCl_4/Ar$. High aspect ratio fins with smooth sidewalls are obtained. To further improve the quality of the sidewalls and shrink the fin width, digital etch is used. Through this process flow, we have demonstrated FinFETs with $L_{g=20}$ nm and fin width as narrow as 7 nm with high yield. Good electrostatic characteristics are obtained in a wide range of device dimensions. In devices with 7 nm fin width, record channel aspect ratio, and transconductance per unit footprint are obtained.**

***Index Terms*—FinFET, III-V CMOS.**

I. INTRODUCTION

InGaAs is a promising channel material candidate for CMOS technologies beyond the 7 nm node [1]–[3]. In this dimensional range, only high aspect-ratio (AR) 3D transistors with a fin or nanowire configuration can deliver the necessary performance. Impressive InGaAs FinFET prototypes have recently been demonstrated [4]–[6]. However, unlike planar InGaAs MOSFETs [7], their performance is still rather unimpressive as compared to Si technology. There are many challenging issues that are unique to FinFETs and that have yet to be tackled. In most demonstrations to date, the fin width in III-V devices is greater than 15 nm. At the point of insertion of this technology, sub-10 nm fin width and steep sidewalls will be required. In addition to the relatively wide fins, most InGaAs FinFETs prior to the work of these authors feature channel-height-to-fin-width aspect ratio (H_c/W_f) of at most 2. This implies a poor use of the footprint of the device. In contrast, state-of-the-art Si FinFETs feature sub-10 nm fin width and a channel aspect ratio in excess of 5 [8].

With the goal of exploring the ultimate potential of InGaAs FinFETs, we have developed a self-aligned recessed-gate process for scaled transistors that emphasizes scalability, performance and manufacturability by making use of dry fin etching, digital etch and Si-compatible materials. For the first time, our work explores the sub-10 nm fin width regime of InGaAs FinFETs. This paper is an augmented version of a recent conference presentation on this topic [9].

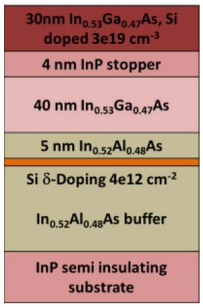

Fig. 1. Starting heterostructure.

II. FABRICATION PROCESS

The starting heterostructure used in our work is sketched in Fig. 1. On an InP substrate, an InAlAs buffer layer is first grown that incorporates a Si δ-doping layer with a sheet concentration of $4x10^{12}$ cm^{-2} placed 5 nm below the channel. The channel is InGaAs lattice matched to InP. The cap consists of heavily-doped Si:InGaAs and an undoped InP etch stopper. Our heterostructure is MBE grown by IntelliEpi.

Our device fabrication process integrates a number of features developed in our group over the last few years [9]–[13] and summarized in Fig. 2. The process starts with sputtering of a low-ρ ($R_{sh} = 5\Omega/\square$) W/Mo ohmic contact bilayer (Mo at bottom) on the as-grown epitaxial structure. This contact-first approach yields outstanding contact resistance in planar devices [10], [13]. The metal stack is then covered by CVD SiO_2. This is used as a hard mask for gate recess and remains on the final device as a vertical spacer.

After E-beam gate patterning, the SiO_2 hard mask and W/Mo contact stack are etched by anisotropic RIE using CF_4:H_2 and SF_6:O_2 chemistries, respectively (Fig. 3) [10].

Manuscript received July 10, 2017; revised August 13, 2017; accepted September 5, 2017. Date of publication September 15, 2017; date of current version October 27, 2017. This work was supported in part by DTRA under Grant HDTRA1-14-1-0057, in part by Lam Research, NSF (E3S STC) under Grant 0939514, and in part by the Korea Institute of Science and Technology. This paper is an augmented version of a work presented at Compound Semiconductor Manufacturing Technology Conference (CS MANTECH), Indian Wells, CA, AZ, May 22-25, 2017 (Ref. 9). *(Corresponding author: A. Vardi.)*

A. Vardi, J. Lin, W. Lu, X. Zhao, and J. A. del Alamo are with the Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: alonva@mit.edu).

A. Fernando-Saavedra is with the ISOM and Departamento de Ingeniería Electrónica, ETSI Telecomunicación, Universidad Politécnica de Madrid, 28040 Madrid, Spain (e-mail: amalia.fernando@isom.upm.es).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TSM.2017.2753141

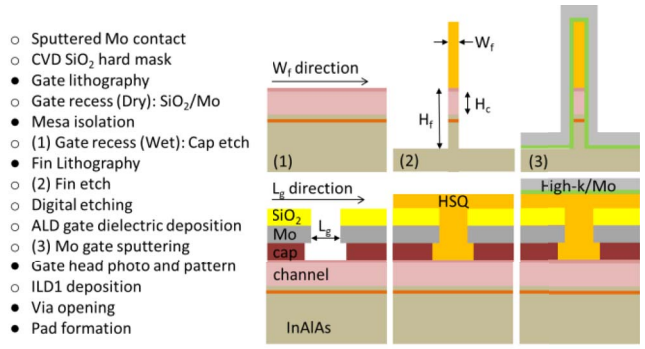

Fig. 2. Left: InGaAs FinFET process flow. Filled circles represent lithography steps. Right: Device schematic at the points in the process marked by numbers. Top (bottom) vignettes are cross sections across (along) the fin direction.

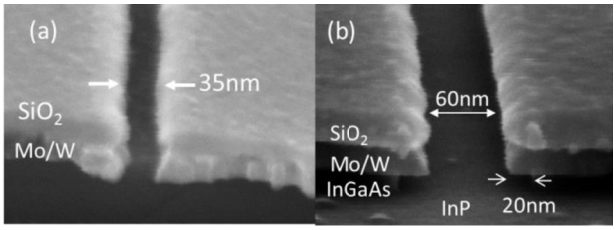

Fig. 3. Pictures at gate recess – (a) after dry etch of SiO_2 and Mo in a device with $L_g = 35$ nm; (b) after subsequent wet etch of InGaAs in $L_g = 60$ nm device. After the wet etch, the cap is pulled back ~20 nm on each side.

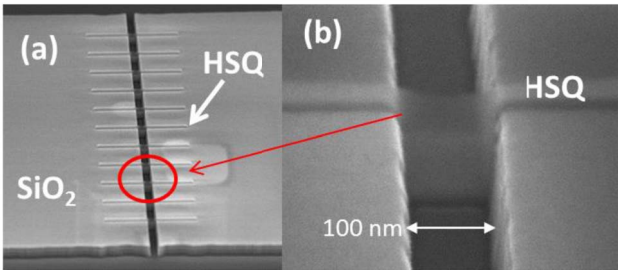

Fig. 4. (a) Array of fins etched in the device recess area; (b) higher magnification of a single fin. The HSQ in the recess area is thicker due to the HSQ planarization property.

F-based RIE stops at the III-V surface. After a mesa definition step, the highly conductive cap is removed using a citric-acid based wet etchant. This process is selective to InGaAs and stops on the undoped InP stopper. The isotropic wet etch pulls back the InGaAs cap underneath the W/Mo contact stack a distance of about 20 nm, as shown in Fig. 3.

With the cap removed, a thin layer (2-3 nm) of Si_3N_4 is deposited by CVD as an adhesion layer for the subsequent fin etch mask which consists of 40 nm thick hydrogen silsesquioxane (HSQ). The overall result is a composite hard mask made out of CVD SiO_2 and HSQ that defines the fins and the S/D area.

The fins are then etched in inductive coupled plasma (ICP) using a $BCl_3/SiCl_4/Ar$ chemistry [14]. This yields fins as narrow as 15 nm with an aspect ratio of ~10 (Fig. 4). The fin etch depth (H_f in Fig. 2) is 170-200 nm and they are highly vertical in the top ~70 nm.

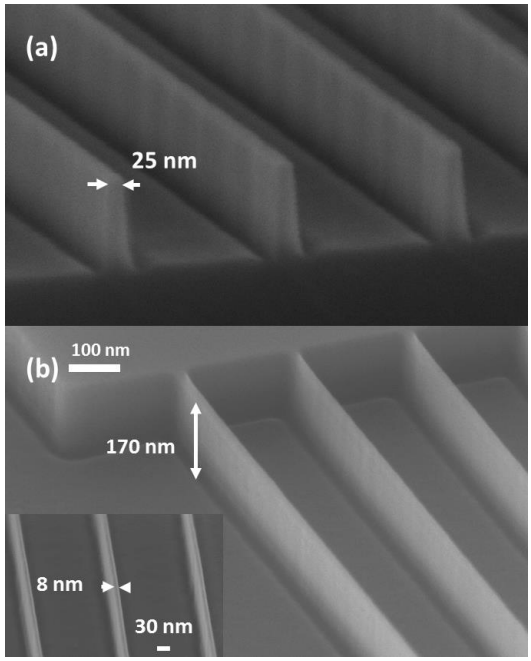

Fig. 5. Fin-etch test structures: (a) cleaved fins as etched; (b) tilted view and top view (inset) of fins after 3 cycles of digital etch.

To further thin down the fins and smooth the sidewalls, we perform several cycles of digital etch (DE) [15] using dry oxidation and H_2O:H_2SO_4 oxide removal (etch rate ~1 nm/cycle for one side, ~2 nm/cycle for the fin width) (Fig. 5). After the last DE cycle, a fresh semiconductor surface is exposed in a final H_2SO_4 cleaning step. This is immediately followed by ALD of 2.2 nm of HfO_2 as gate dielectric and Mo gate metal sputtering (Fig. 6). The frontend is completed by gate metal definition, using SF_6:O_2 dry etch. The gate metal covers completely the fins and overlaps with the source and drain regions. About 30 nm of the SiO_2 hard mask separate the S/D and the gate metals (marked in Fig. 6a).

The backend comprises of inter-level dielectric (ILD) deposition, via opening and pad formation. More details on the backend below.

In our process, the HSQ used to define the fins, is spun on a surface with substantial topography (there is a height difference of 80 nm in the recessed area that arises from the combined thickness of SiO_2, W/Mo and InGaAs etched cap). As a consequence, the final thickness of the HSQ fin etch mask is greatly affected by the planarization properties of HSQ [16]. Since HSQ has low viscosity at relatively low temperatures (20-100 °C), it tends to reflow. Consequently, the thickness of the HSQ in the recessed area almost equals that of the recessed trench depth. This can be seen in Fig. 4(b) and also in Fig. 7 that compares the HSQ thickness at the overlap area and in the trench after the fins have been etched. Since the HSQ after development tends to be thinner for narrower lines, as seen in Fig. 6(c) (dashed lines), our approach is stable down to 15 nm wide fins (after RIE). We can reach below this fin width through digital etch.

A key aspect of our process is that the HSQ that defines the fin etch is kept in place. This makes our FinFETs *double-gate MOSFETs* with carrier modulation only on the sidewalls.

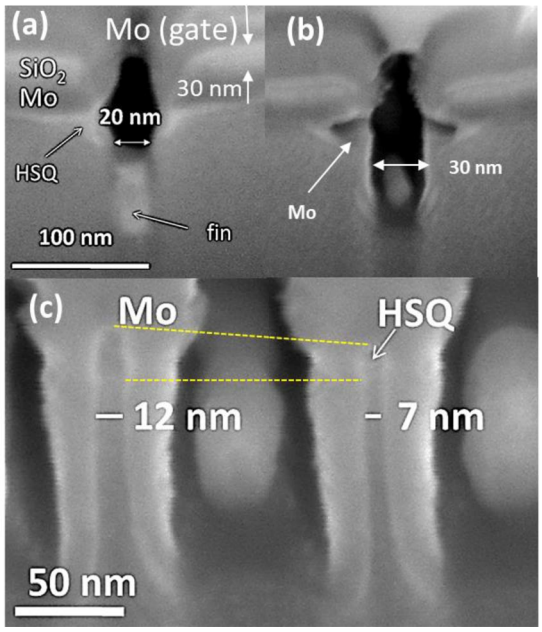

Fig. 6. FIB cross-section of finished device from source to drain: (a) along fin and (b) between fins. (c) Cross-section FIB of two completed fin test structures.

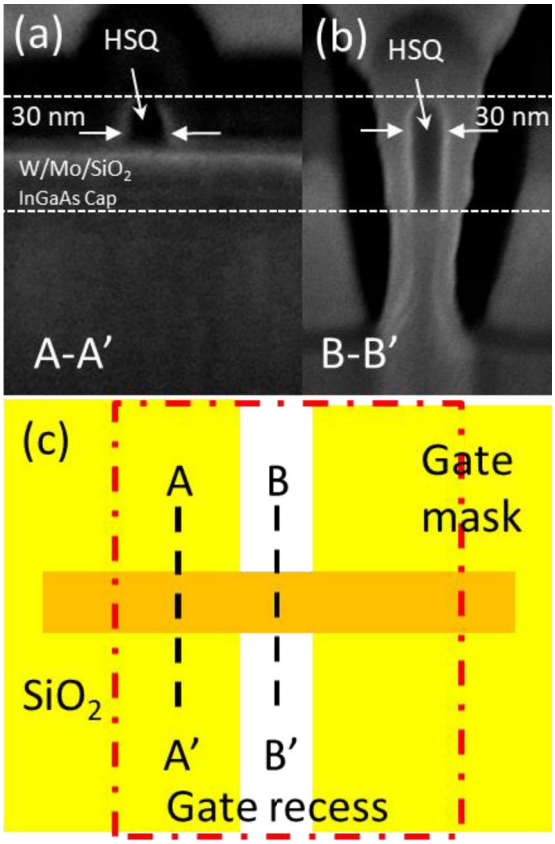

Fig. 7. FIB cross sections of a finished device across the fin width direction under the gate mask. (a) Corresponds to Section AA' under the SiO_2 spacer right next to the intrinsic region of the device. (b) Corresponds to Section BB' in the intrinsic portion of the device. (c) Schematic of the device in top view showing the positions of the cross sections. Dash lines in (a) and (b) indicate the total height of the HSQ in the intrinsic region and the alignment between the two cross sections.

While theoretically inferior to trigate designs, practically, the greater simplicity of the double-gate FinFET fabrication process allows us to aggressively scale all device dimensions and implement a robust self-aligned flow with high process tolerance and yield. This ultimately results in significantly better performance than prior InGaAs Trigate MOSFET demonstrations, as discussed below. In addition, for high channel-height to fin-width aspect ratio (AR = H_c/W_f), a top gate yields diminishing returns [17].

Our entire front-end fabrication (before pads) closely follows Si CMOS-compatibility requirements and is completely lift-off free and Au-free. The overall process has a very low thermal budget with a maximum temperature of 300°C set by the SiO_2 CVD deposition.

Devices with fin widths ranging from 7 to 22 nm, on a fin pitch of 200 nm were fabricated with a high yield. The gate lengths range from 20 to 600 nm. FIB cross-sections of a finished device ($L_g = 20$ nm) along the fin length direction and between the fins are shown in Fig. 6(a) and (b), respectively. Due to the underlap of the cap, the separation between source and drain between the fins is ~10 nm wider than the length of the fins. FIB cross sections of devices with $W_f = 7$ nm and 12 nm are show in Fig. 6(c).

III. Off-Current and EOT Optimization

The active layer in our device is grown over semi insulating InAlAs and the fins are cut all the way into it. In spite of this, the thin gate oxide provides for poor isolation in the extrinsic portion of the device. To reduce buffer leakage between the gate and the source/drain pads, it is necessary to separate the large metal lines and pads from the buffer layer by adding ILD. Two critical leakage path are likely: 1) through the bottom of the pads and 2) through the mesa sidewalls.

TABLE I
Process Splits (A-D) for ILD and Gate Oxide EOT Optimization. Gate Leakage Is Given at $V_{GS} = 0.5$ V and $V_{DS} = 50$ mV

	ILD type	ILD Thickness [nm]	Gate Oxide	EOT [nm]	J_g [A/cm^2]
A	Al_2O_3 ALD	2.8	Al_2O_3	2.8	30
B	SiO_2 CVD	30	Al_2O_3/HfO_2	1	1.5
C	TEOS CVD	30	HfO_2	0.8	0.1
D	TEOS CVD	30	HfO_2	0.6	340

Both are sketched in Fig. 8(a). To enable further scaling of EOT while maintaining low gate leakage our process includes ILD deposited before final via opening. This is sketched in Fig. 8(b).

The gate leakage of different process splits is summarized in Table I and shown in Fig. 8(c) for $L_g = 300$ nm devices. Since in our device there are no spacers, the sidewalls of the source and drain between the fins are gated (Fig. 6(b)). Therefore, the gate leakage is normalized by the total active sidewall area, $2H_c \cdot (L_g + W_{nf}) \cdot N_f$, where W_{nf} is the spacing between the fins and N_f is the number of fins.

Split A does not have ILD, rather, it relies for isolation on the high-k gate oxide that is deposited on the sample during the fabrication of the gate stack. This is indicated

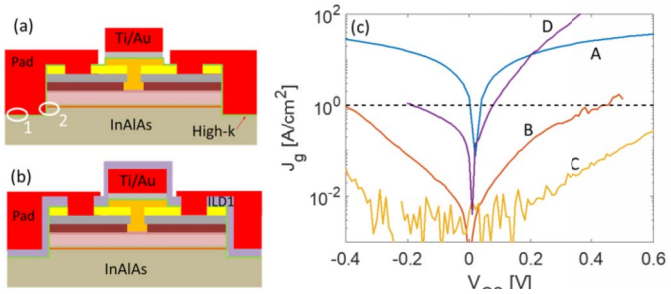

Fig. 8. Schematics of finished device cross section along the fin direction without (a) and with (b) interlevel dielectric layer. In (a), two circles indicate buffer leakage paths through the large area pads and the mesa sidewalls. (c) Gate leakage obtained for the different process splits depicted in Table I.

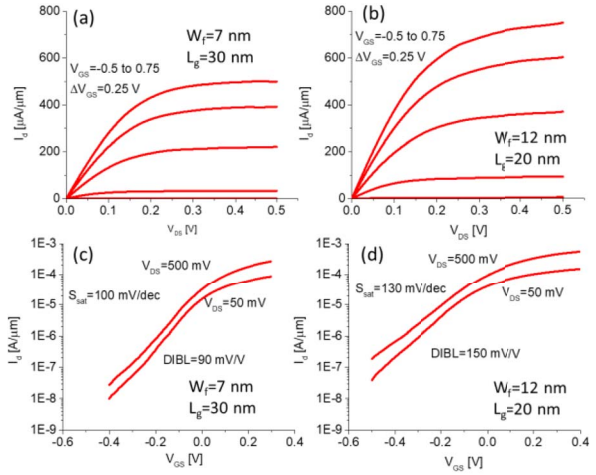

Fig. 9. Output (a,b) and subthreshold (c,d) characteristics of a FinFET with $W_f = 7$, 12 nm (a,c) and $L_g = 30$, 20 nm (b,d).

in Fig. 8(a). Split B includes an ILD made out of 30 nm of CVD SiO_2. A reduced gate leakage was obtained even though the gate dielectric was thinned down to an EOT of 1 nm. To improve sidewall coverage, we replaced the SiO_2 by TEOS. This allowed further scaling of EOT to 0.8 nm while maintaining gate leakage below 1 A/cm^2 across a wide V_{GS} range (split C). Further reduction of EOT to 0.6 nm with the same ILD gave much higher gate current (split D). In our final process, we settled on split C. These results are comparable (but slightly higher) than the gate leakage current obtained on planar InGaAs MOSFETs with similar ILD and gate oxide EOT [11].

IV. Electrical Characteristics

The electrical characteristics of typical devices with $L_g = 30$, 20 nm and $W_f = 7$, 12 nm (AR $= H_c/W_f = 5.7, 3.3$), are shown in Fig. 9. Well-behaved characteristics and good sidewall control are demonstrated. The device R_{on} is 320, 300 $\Omega \cdot \mu$m and a peak g_m of 900, 1250 μS/μm is obtained at $V_{DS} = 0.5$ V (Fig. 10). Consistent with the double-gate nature of our devices and following common practice, all figures of merit have been normalized by the conducting gate periphery which, in our case, is two times the channel height. The subthreshold characteristics of the same device (Fig. 9b) indicate

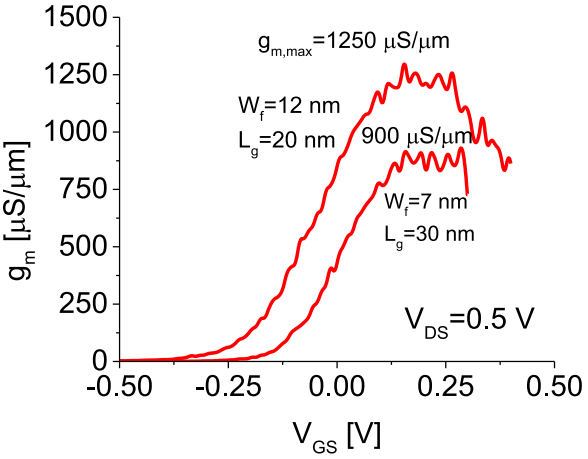

Fig. 10. Saturated g_m characteristics of the FinFETs of Fig. 9.

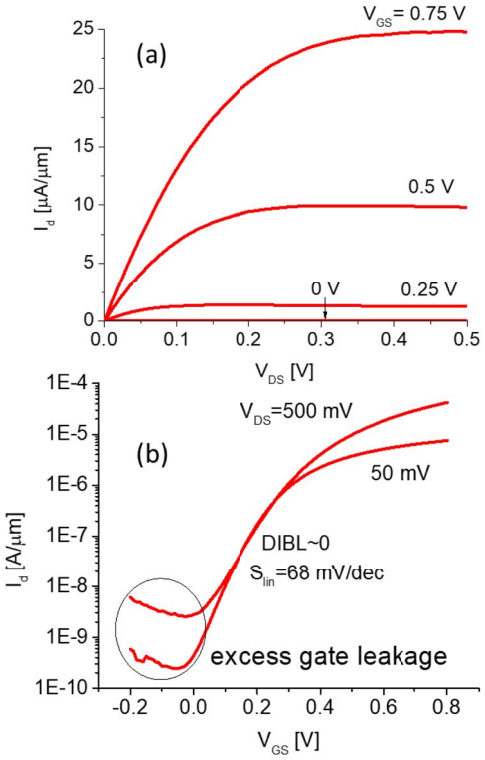

Fig. 11. (a) Output and (b) subthreshold characteristics of device with $W_f = 22$ nm and $L_g = 2\mu$m. A nearly ideal $S_{lin} = 68$ mV/dec is obtained.

a saturated subthreshold swing, S_{sat}, of 100, 130 mV/dec and DIBL of 90, 150 mV/V at 0.5 V, respectively.

In devices with $L_g = 30$ nm and $W_f = 22$ nm, a peak g_m of 1500 μS/μm is obtained. For $L_g = 2\mu$m and $W_f = 22$ nm, S_{lin} at $V_{DS} = 50$ mV is as low as 68 mV/dec (Fig. 11), indicating a high quality interface between the semiconductor sidewall and the high–k gate oxide [18]. At negative V_{GS} the subthreshold characteristics are governed by gate leakage.

The scaling behavior of our FinFET was studied in detail in [18]. Classic EOT and L_g scaling behavior was demonstrated for wide-fin devices. In contrast, Fig. 12 shows the scaling of g_m and saturated S with L_g and W_f. While g_m

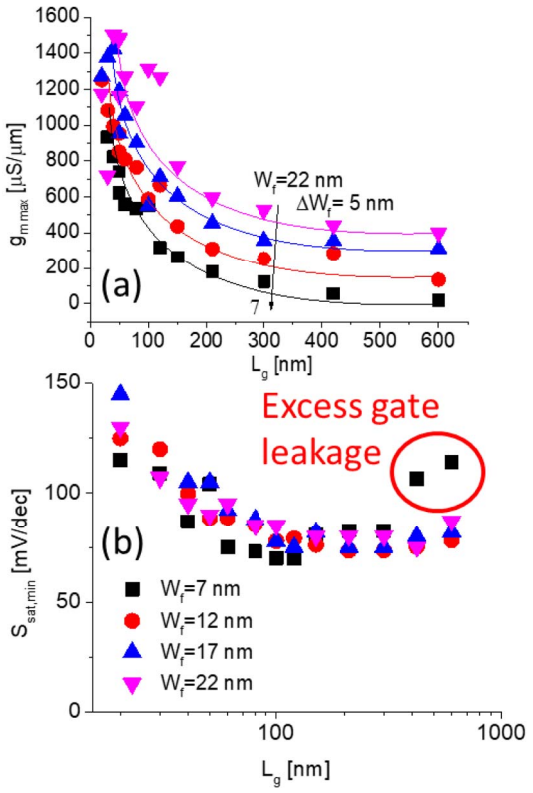

Fig. 12. g_m and S_{sat} vs. L_g for different W_f. Both, g_m and S_{sat} are given at $V_{DS} = 0.5$ V. Non-ideal fin-width scaling is evident. The high subthreshold swing for long L_g transistors is due to excessive gate leakage current.

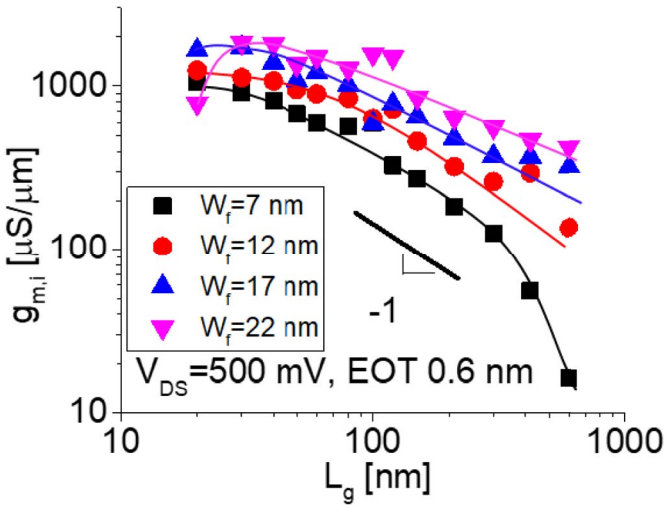

Fig. 13. Intrinsic $g_{mi,max}$ scaling with L_g for different W_f.

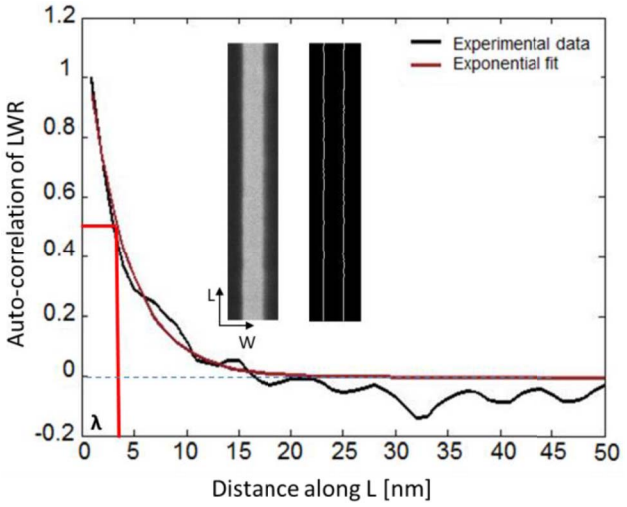

Fig. 14. Autocorrelation of LWR, for $W_f = 35$ nm, inset shows top view SEM image of fin with $W_f = 35$ nm and the extracted LER.

increases as L_g scales down, a clear reduction of g_m is observed with W_f scaling. This reduction is unexpected since fin width scaling should enhance gate control over the fin channel and increase g_m. In addition, the saturated subthreshold swing shows weak dependence on fin width. The high subthreshold swing for transistors with $W_f = 7$ nm and $L_g > 300$ nm (marked with red circle in Fig. 12(b)) is due to excessive gate leakage current. This indicates that the fin sidewall quality degrades for long fins. These are all manifestations of improper fin-width scaling.

In order to understand the origin of the poor fin-width scaling, we have extracted the intrinsic transconductance g_{mi}. This is derived from $g_{mi} = g_m/(1\text{-}R_s.g_m)$ where R_s is taken as $1/2R_{sd}$ as extracted from R_{on} measurements vs. L_g and extrapolation to $L_g = 0$ [18]. For all W_f, R_s is in the range of 50-70 $\Omega \cdot \mu$m. Fig. 13 shows the peak value of g_{mi} as a function of L_g for the different fin widths. For all devices with $L_g > 100$ nm, g_{mi} increases rapidly as L_g shrinks. Below $L_g = 100$ nm, g_{mi} scales much more weakly with L_g as a result of short-channel effects. The degradation of g_{mi} with W_f is observed across the entire L_g span and it is more prominent for long-channel devices. This suggests that the source of g_{mi} degradation is intrinsic. The most likely candidates are poor sidewall characteristics in the form of excessive interface state density or sidewall roughness, or line-edge roughness from e-beam lithography and RIE processes used to define the fins. Understanding and addressing these issues is crucial for the eventual success of this technology.

V. Discussion

We have studied the line-edge roughness (LER) of our fins. LER refers to the fluctuation of the fin edges. These fluctuations are transferred from the fin etch mask (HSQ) during fin etch. We have also studied fin-width roughness (LWR). This refers to the fluctuation of the width of the fin.

To study fin LER and LWR, we fabricated long (100 μm) fins with W_f ranging from 20 to 35 nm following an identical process as in the real devices. The HSQ is patterned using e-beam lithography, using a spot size of 2.5 nm along the fins (L direction in Fig. 14 inset). Following fin etch, the HSQ is removed using BOE. No digital etch was performed. LER and LWR are obtained from top-view SEM image analysis (inset of Fig. 14). The fin edges are detected using a home-made MATLAB program which uses the Canny algorithm [19] to detect the fin edges. The same program also calculates the autocorrelation function. From this analysis, the standard deviation (σ) and correlation length (λ) of edges and fin width fluctuations are calculated.

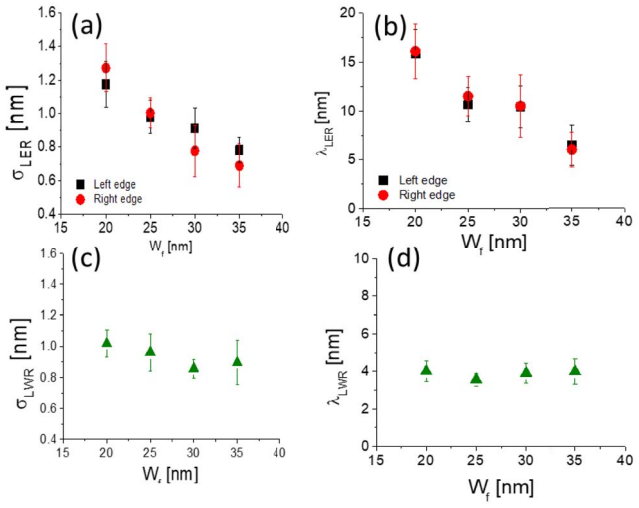

Fig. 15. Standard deviation and correlation length of LER (a,b) and LWR (c,d), respectively, as a function of W_f. data collected from total fin length of 1 μm.

The autocorrelation function can be fitted by an exponential where the correlation length (λ) is defined at 0.5 (Fig. 14) [20], [21]. Fig. 15 shows the results of the analysis. σ_{LER} and λ_{LER} (a-b) exhibit the same trend: they both increase as W_f scales down. Interestingly, σ_{LWR} and λ_{LWR} (c-d) are significantly smaller and almost W_f independent. The increased LER with W_f scaling may be attributed to the fin patterning scheme. Since in wider fins there are more beam passes, a certain degree of averaging takes place that smooths the sidewalls. The origin of the high correlation between the two edges is still unclear and requires further research. However, the short correlation length implies that even our shortest gate length devices suffer from LER. Also, this becomes exacerbated as L_g increases, as seen in Fig. 13 by the rapid drop in g_{mi} for $W_f = 7$ nm.

VI. Benchmarking

InGaAs FinFETs to date have indeed demonstrated excellent short-channel effects, as illustrated in Fig. 16. This figure shows linear subthreshold swing in experimental devices graphed against the ratio of L_g to the characteristic scaling length for electrostatics [22]. The experimental data approach the expected ideal scaling behavior [23]. This is what makes the FinFET architecture a very promising one for deeply scaled devices.

Regarding ON-state characteristics, Fig. 17 benchmarks peak g_m of InGaAs FinFETs published to date [4]–[6], [24]–[31] as a function of fin width. The same data is graphed in two different ways: the conventional approach (Fig. 16(a)), which normalizes g_m by the width of the conducting gate periphery; and an alternative method, where the same data are normalized by the fin width (Fig. 16(b)). The latter approach is relevant, because it relates to transistor density, which, in the end, is what Moore's Law is all about. A winning FinFET should be capable of conducting a lot of current standing on a minimum footprint. Both graphs include estimations (green symbols)

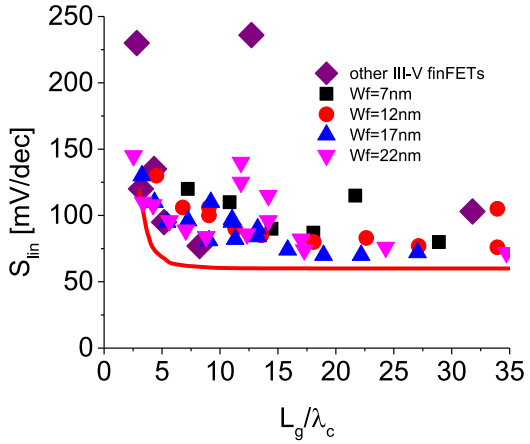

Fig. 16. Linear subthreshold swing (low V_{DS}) vs. ratio of gate length to electrostatic scaling length in experimental InGaAs FinFETs. For reference, the red line indicates ideal electrostatic behavior [21].

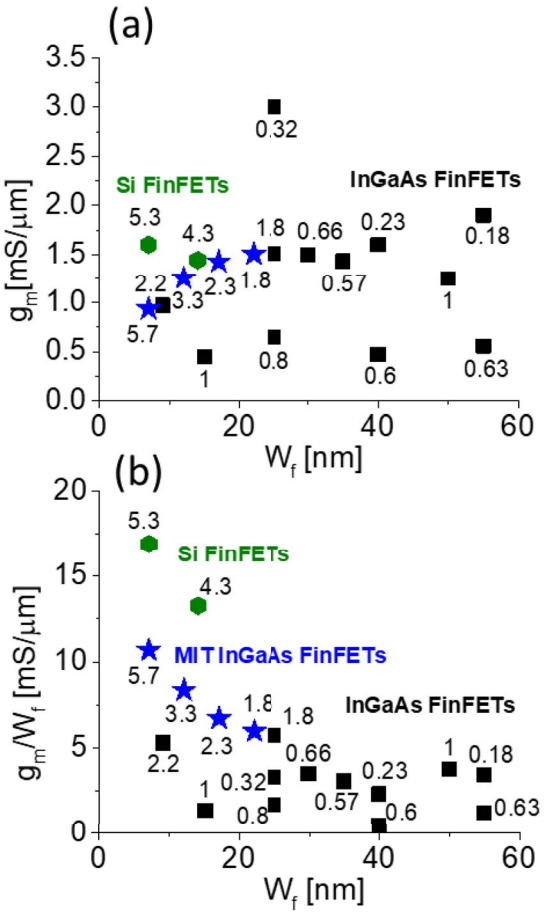

Fig. 17. Benchmark of maximum g_m vs. W_f for InGaAs FinFETs and state-of-the-art Si FinFETs. (a) g_m normalized by conducting gate periphery. (b) g_m normalized by fin footprint. The numbers next to each data point represent the aspect ratio of the conducting channel (height over width).

from selected state-of-the-art silicon FinFETs (22 nm and 14 nm CMOS from Intel [30], [31]), along with the best of our recently published results in blue stars [18], [27]. Next to etch data point the channel aspect ratio (channel height over fin width) is indicated.

When normalized to gate periphery (Fig. 16(a)), Si and InGaAs FinFETs show equivalent performance (there is a recent result with significantly higher g_m on a device with a modest channel aspect ratio [28]). However, it is important to note that, with the exception of the devices presented in this work (blue stars), the fin width and aspect ratio of InGaAs FinFETs in the literature is far from that of Si FinFETs and from what is required for beyond 7-nm applications.

On the other hand, when normalizing to fin footprint (Fig. 16(b)), a large gap between Si and InGaAs transistors is revealed. Our devices [18], [27] contribute to bridging this gap due to narrow fins and relatively efficient use of sidewall conductivity. Our devices yield 3x more transconductance per channel footprint than the best planar InGaAs MOSFETs [7]. Part of the gap between InGaAs and Si FinFETs is due to the different operating voltages (0.5 V for InGaAs, 0.8 V for Si). However, correcting for this still leaves a sizeable difference. Clearly, more work is ahead before InGaAs FinFETs match and eventually exceed the performance of Si FinFETs.

VII. Conclusion

We demonstrate self-aligned InGaAs FinFETs with extremely thin fins (down to 7 nm), high channel aspect ratios (as high as 5.7), short gate lengths (down to 20 nm) and excellent performance. When scaled by the fin footprint, our transistors improve the state of the art by nearly a factor of three, suggesting effective channel charge control from the sidewalls of very thin, high aspect-ratio fins.

Acknowledgment

Device fabrication was carried out at the Microsystems Technology Laboratories and the Electron Beam Lithography Facility at MIT. The help of Dr. T. Yu in line edge roughness analysis is gratefully acknowledged.

References

[1] J. A. del Alamo *et al.*, "InGaAs MOSFETs for CMOS: Recent advances in process technology," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, USA, 2013, pp. 2.1.1–2.1.4.

[2] J. A. del Alamo *et al.*, "Nanometer-scale III-V MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 4, no. 5, pp. 205–214, Sep. 2016.

[3] H. Riel, L.-E. Wernersson, M. Hong, and J. A. del Alamo, "III–V compound semiconductor transistors—From planar to nanowire structures," *MRS Bull.*, vol. 39, no. 8, pp. 668–677, Aug. 2014.

[4] R. Oxland *et al.*, "InAs FinFETs with $H_{fin} = 20$ nm fabricated using a top–down etch process," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 261–264, Mar. 2016.

[5] V. Djara *et al.*, "An InGaAs on Si platform for CMOS with 200 mm InGaAs-OI substrate, gate-first, replacement gate planar and FinFETs down to 120 nm contact pitch," in *Proc. Symp. VLSI Technol. (VLSI Technology)*, Kyoto, Japan, 2015, pp. T176–T177.

[6] M. L. Huang *et al.*, "High performance In0.53Ga0.47As FinFETs fabricated on 300 mm Si substrate," in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, 2016, pp. 1–2.

[7] J. Lin, X. Cai, Y. Wu, D. A. Antoniadis, and J. A. del Alamo, "Record maximum transconductance of 3.45 mS/μm for III-V FETs," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 381–384, Apr. 2016.

[8] J. A. del Alamo *et al.*, "Nanometer-scale III-V MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 4, no. 5, pp. 205–214, Sep. 2016.

[9] A. Vardi, J. Lin, W. Lu, X. Zhao, and J. A. del Alamo, "A Si-compatible fabrication process for scaled self-aligned InGaAs FinFETs," in *Proc. Compound Semicond. Manuf. Technol. Conf. (CS MANTECH)*, Indian Wells, CA, USA, May 2017.

[10] J. Lin, T.-W. Kim, D. A. Antoniadis, and J. A. del Alamo, "A self-aligned InGaAs quantum-well metal–oxide–semiconductor field-effect transistor fabricated through a lift-off-free front-end process," *Appl. Phys. Exp.*, vol. 5, no. 6, May 2012, Art. no. 064002.

[11] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Sub-30 nm InAs quantum-well MOSFETs with self-aligned metal contacts and sub-1 nm EOT HfO2 insulator," in *Proc. Int. Electron Devices Meeting*, San Francisco, CA, USA, 2012, pp. 32.1.1–32.1.4.

[12] J. Lin, X. Zhao, T. Yu, D. A. Antoniadis, and J. A. del Alamo, "A new self-aligned quantum-well MOSFET architecture fabricated by a scalable tight-pitch process," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, USA, 2013, pp. 16.2.1–16.2.4.

[13] W. Lu, A. Guo, A. Vardi, and J. A. del Alamo, "A test structure to characterize nano-scale ohmic contacts in III-V MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 2, pp. 178–180, Feb. 2014.

[14] X. Zhao and J. A. del Alamo, "Nanometer-scale vertical-sidewall reactive ion etching of InGaAs for 3-D III-V MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 521–523, May 2014.

[15] J. Lin, X. Zhao, D. A. Antoniadis, and J. A. del Alamo, "A novel digital etch technique for deeply scaled III-V MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 440–442, Apr. 2014.

[16] H. J. Lee *et al.*, "Application of HSQ (hydrogen silsesquioxane) based SOG to pre-metal dielectric planarization in STC (stacked capacitor) DRAM," in *Symp. VLSI Technol. Dig. Tech. Papers*, Honolulu, HI, USA, 1996, pp. 112–113.

[17] S.-H. Kim, J. G. Fossum, and V. P. Trivedi, "Bulk inversion in FinFETs and implied insights on effective gate width," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 1993–1997, Sep. 2005.

[18] A. Vardi and J. A. del Alamo, "Sub-10-nm Fin-width self-aligned InGaAs FinFETs," *IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1104–1107, Sep. 2016.

[19] J. Canny, "A computational approach to edge detection," *IEEE Trans. Pattern Anal. Mach. Intell.*, vol. PAMI-8, no. 6, pp. 679–698, Nov. 1986.

[20] X. Jiang, R. Wang, T. Yu, J. Chen, and R. Huang, "Investigations on line-edge roughness (LER) and line-width roughness (LWR) in nanoscale CMOS technology: Part I—Modeling and simulation method," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3669–3675, Nov. 2013.

[21] T. Yu *et al.*, "Investigation of nanowire line-edge roughness in gate-all-around silicon nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2864–2871, Nov. 2010.

[22] N. Agrawal Y. Kimura, R. Arghavani, and S. Datta, "Impact of transistor architecture (bulk planar, trigate on bulk, ultrathin-body planar SOI) and material (silicon or III–V semiconductor) on variation for logic and SRAM applications," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3298–3304, Oct. 2013.

[23] C.-W. Lee, S.-R.-N. Yun, C.-G. Yu, J.-T. Park, and J.-P. Colinge, "Device design guidelines for nano-scale MuGFETs," *Solid State Electron.*, vol. 51, no. 3, pp. 505–510, 2007.

[24] M. Radosavljevic *et al.*, "Electrostatics improvement in 3-D tri-gate over ultra-thin body planar InGaAs quantum well field effect transistors with high-K gate dielectric and scaled gate-to-drain/gate-to-source separation," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2011, pp. 33.1.1–33.1.4.

[25] S.-H. Kim *et al.*, "High performance tri-gate extremely thin-body InAs-On-insulator MOSFETs with high short channel effect immunity and V_{th} tunability," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1354–1360, May 2014.

[26] A. V. Thathachary *et al.*, "Indium arsenide (InAs) single and dual quantum-well heterostructure FinFETs," in *Proc. Symp. VLSI Technol. (VLSI Technol.)*, Kyoto, Japan, Jun. 2015, pp. T208–T209.

[27] A. Vardi, J. Lin, W. Lu, X. Zhao, and J. A. del Alamo, "High aspect ratio InGaAs FinFETs with sub-20 nm fin width," in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, 2016, pp. 1–2.

[28] C. B. Zota, F. Lindelow, L. E. Wernersson, and E. Lind, "InGaAs tri-gate MOSFETs with record on-current," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2016, pp. 3.2.1–3.2.4.

[29] X. Sun *et al.*, "High performance and low leakage current InGaAs-on-silicon FinFETs with 20 nm gate length," in *Proc. IEEE Symp. VLSI Technol.*, Kyoto, Japan, 2017, pp. T40–T41.

[30] C.-H. Jan *et al.*, "A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications," in *Proc. IEDM*, San Francisco, CA, USA, Dec. 2012, pp. 3.1.1–3.1.4.

[31] S. Natarajan *et al.*, "A 14nm logic technology featuring 2^{nd}-generation FinFET, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 SRAM cell size," in *Proc. IEDM*, San Francisco, CA, USA, Dec. 2014, pp. 3.7.1–3.7.3.

Authors' photographs and biographies not available at the time of publication.